

IN THE CLAIMS

Please cancel claim 10 without prejudice.

All pending claims remaining in the application are set forth below.

1. (Currently amended) A digital signal processor comprising:
 - an analog front end including an analog-to-digital converter for receiving an input signal;
 - a digital base-band processor having a latency period for detecting a signal, coupled to the analog front end;
 - a shift register for tracking data representing the relative amplitude of samples of the input signal for a period at least equal to the latency period;
 - a gain control counter, coupled to the shift register, controlled by a current relative amplitude of one of the samples of the input signal and an output from the shift register representing the relative amplitude of one of the samples taken at an earlier time, the control ceasing once the base-band processor detects a signal of a predetermined threshold from the analog front end; and
 - a gain control circuit coupled to the counter for controlling gain of the input signal.
2. (Canceled)
3. (Canceled)

4. (Previously amended) The digital signal processor of claim 1 wherein the gain control circuit includes a comparator for comparing a count in the gain control counter with a predetermined count and based upon the results of the comparison, adjusts the gain of the input signal.
5. **(Canceled)**
6. (Previously amended) The digital signal processor of claim 23 wherein the first shift register is coupled to a first comparator which compares samples of the input signal with a lower threshold level.
7. (Original) The digital signal processor of claim 6 wherein the second shift register is coupled to a second comparator which compares samples of the sampled input signal with an upper threshold level.
8. (Original) The digital signal processor of claim 7 wherein the first and second shift registers each have a number of stages approximately equal to the number of samples occurring during the latency period.
9. (Original) The digital signal processor defined by claim 8 wherein the gain control counter comprises a first gain control counter and a second gain control counter, the first gain control counter being controlled by the first comparator and the first shift register and the second gain control counter being controlled by the second comparator and the second shift register.
10. **(Canceled)**

11. (Currently amended) The digital signal processor defined by claim [[10]] 9 including a first logic circuit coupled to receive a most significant bit from the first shift register and an output of the first comparator for providing a count-up and count-down signal to the first gain control counter.
12. (Original) The digital signal processor of claim 11 including a second logic circuit coupled to receive a most significant bit from the second shift register and an output of the second comparator for providing a count-up and count-down signal to the second gain control counter.
13. (Currently amended) The digital signal processor of claim [[10]] 9 including a third comparator for comparing a current count in the first gain control counter with a first predetermined count and for providing an output for increasing gain if the current count is less than the first predetermined count.
14. (Currently amended) The digital signal processor of claim [[11]] 13 including a fourth comparator for comparing the current count in the second gain control counter with a second predetermined count and for decreasing gain if the current count is greater than the second predetermined count.

Claims 15-18 (Canceled)

19. (Currently amended) A method for controlling gain in a digital signal processor comprising:

tracking data representing the relative amplitude of an input signal;
controlling the gain by considering a current amplitude and a prior
amplitude from the tracked data taken earlier in time; and
ceasing to consider the tracked data once the input signal is detected.

20. (Canceled)

21. (Previously amended) The method defined by claim 19 wherein the tracking step comprises, recording first bits representing samples of the input signal that exceed a first predetermined threshold and second bits representing samples of the input signal that are less than a second predetermined threshold.

22. (Currently amended) The method defined by claim 21 wherein the processor has a signal detection latency period and the ~~tracked data~~ step of tracking data continues is for a period at least as long as the latency period.

23. (Currently amended) A digital signal processor comprising:

an analog front end including an analog-to-digital converter for receiving an input signal;

a digital base-band processor having a latency period for detecting a signal, coupled to the analog front end;

a first shift register and a second shift register for tracking data representing the relative amplitude of samples of the input signal;

a gain control counter controlled by a current relative amplitude of sample of the input signal and an output from the shift registers representing a relative amplitude of a sample taken earlier in time, coupled to the shift registers; and

a gain control circuit coupled to the counter for controlling gain of the input signal.